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High-end Microelectronics Design

Read-Out Chips Catalog

V032021

Product lineup

About Weeroc

Weeroc is a fabless microelectronics company designing and providing front-end read-out chips for most of the particle detector or photodetectors. Weeroc offers off-the-shelf programmable read-out chips and associated support for a fast and successful integration of the read-out chip in user system.

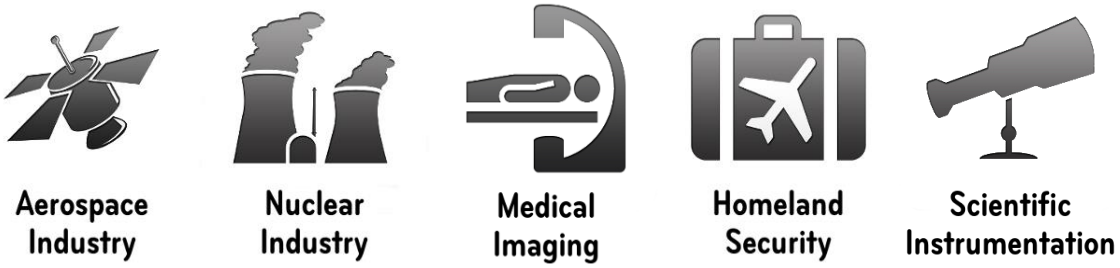
Weeroc designs custom read-out chip on customer request for specific application not covered by programmable component off the shelf.

Weeroc's core of design expertise includes low noise and radiation-hardened mixed signal ASICs.

Weeroc is certified ISO9001 since 2015.

Application Domains

Weeroc ASICs are suitable for most industrial or research application involving photodetector or particle detector read-out.



Dedicated Design

Weeroc can design dedicated ASIC for specific application. Non-recurrent design cost are paid by the final customer who have exclusive access to the design he ordered. Typical microelectronics design is 18 months from requirement specification to tested prototypes.

Integration services

Weeroc provide a dedicated front-end board design service to help our customer build their system if no system of the shelf meet their requirements.

Product lineup

Programmable read-out chip off the shelf

Weeroc offer a full range of product to read-out almost any kind of detectors. The table below describes which read-out chip is suitable for which kind of detectors. Weeroc application engineers can help you choose the best fit for your detector and application.

	SiPM	MA-PMT	PMT	APD	Pin diode	Silicon strips	RPCs	Micromegas GEMS
Maroc 3A	✓	✓	✓					
Catiroc 1	✓	✓	✓					
Citiroc 1A	✓							
Petiroc 2A	✓						✓[1]	
Triroc 1A	✓							
Skiroc 2A				✓	✓	✓		
Gemroc 1				✗	✗	✗		✓

✓ Fully optimized readout - ✓ Compatibility - ✗ Compatibility not fully accessed

[1] Petiroc can read RPCs on the trigger line solely, no compatibility on the energy measurement line

Weeroc products maturity is ranged using technical readiness level (TRL) scale. The Weeroc definition of TRL is described below.

Technology Readiness Level	Description
TRL 1	ASIC project
TRL 2	ASIC in foundry
TRL 3	silicon available
TRL 4	First measurements, minor bug detected
TRL 5	First measurement, conclusive in lab
TRL 6	Application prototype available
TRL 7	Full system using ASIC available
TRL 8	Full system using ASIC running
TRL 9	Full system running ASIC, reliability proven

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Product lineup

	Maroc	Catiroc	Gemroc	Skiroc	Citiroc	Petiroc	Triroc
Prod. Version	3A	1	1	2A	1A	2A	1A
TRL	9	8	9	8	9	6	8
Package*	PQFP240 TFBGA353	TQFP208	PQFP160	BGA400	PQFP160 TFBGA353	TQFP208 TFBGA353	TFBGA353
Detector Compatibility	- MA-PMT, PMT - SiPM, SiPM array	- MA-PMT, PMT	- micromegas - GEMs	- Si PIN diodes - Silicon strips	- SiPM - SiPM array	- SiPM - SiPM array	- SiPM - SiPM array
Optimized readout	MA-PMT	PMT	GEMs	Si PIN diodes	SiPM	SiPM	SiPM
Channel	64	16	64	64	32	32	64
Measurements and operations	- Free running trigger - External trigger - Charge (shaper) - Photon counting - Time (trigger)	- Free running trigger - Ext trigger - Charge (shaper) - Time (trigger) - Time (TDC)	- Free running trigger - Ext trigger - Charge (shaper) - Data 3-level trigger	- Free running trigger - Ext trigger - Charge(shaper) - Time (TDC)	- Free running trigger - Ext trigger - Charge (shaper) - Time (trigger)	- Free running trigger - Charge (shaper) - Time (trigger) - Time (TDC)	- Free running trigger - Charge (shaper) - Time (TDC)
Outputs	- 64 Triggers - Trigger OR - 1 analog multiplexer (charge) - ADC (8/10/12b)	- 16 Triggers - 16 Shapers - Trigger OR - ADC (10b) - TDC (10b)	- Trigger OR - 1 analog multiplexer (charge)	- Trigger OR - 1 analog multiplexer (charge) - ADC (10/12b) - TDC (10/12b)	- 32 triggers - Trigger OR - 1 analog multiplexer (charge)	- 32 triggers - Trigger OR - 1 analog multiplexer (charge) - 1 digital multiplexer (trigger) - ADC (10b) - TDC (10b)	- Trigger OR - analog multiplexer (charge) - 1 digital multiplexer (trigger) - ADC (10b) - TDC (10b)
Input Polarity	Negative	Negative	Negative	Positive	Positive	Negative (optimized) Positive	Negative (optimized) Positive
Applications Main features	Energy meas. SPE application Photon counting rate < 30MHz MA-PMT gain adj.	Energy meas. Time stamping Low dead time Zero suppress data	Energy meas. Time stamping Data readout : 3-level trigger	Energy meas. Time stamping	Energy meas. Time of flight Photon counting Calibration input SPE spectrum Input DAC SiPM HV adjust.	Energy meas. Time of flight Time stamping Photon counting Input DAC SiPM HV adjust.	Energy meas. Time of flight Time stamping Zero suppress data Input DAC SiPM HV adjust.

*QFP packaging will be phased out and replaced with equivalent BGA packaging. Glossary: ADC : Analog to Digital Converter – TDC : Time to Digital Converter

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Maroc 3A

Photomultiplier-tubes read-out chip

MAROC3A is a 64-channel chip designed to readout negative fast input current pulses such as those provided by Multi Anode Photo Multipliers. Each channel provides a 100% trigger rate for signal greater than 1/3 photoelectron (50fC) and a charge measurement up to 30 photoelectrons (~ 5 pC) with a linearity of 2%. The gain of each channel can be tuned between 0 and 4 thanks to an 8-bit variable gain preamplifier allowing to compensate the non- uniformity between detector channels. A slow shaper combined with two Sample and Hold capacitors allows storing the charge up to 5 pC as well as the baseline. In parallel, 64 trigger outputs are obtained thanks to two possible trigger paths: one made of a bipolar or unipolar fast (15 ns) shaper followed by one discriminator for the photon counting and one made with a bipolar fast shaper (with a lower gain) followed by a discriminator to deliver triggers for larger input charges (> 1 pe). The discriminator thresholds are set by two internal 10-bit DACs. A digital charge output is provided by an integrated 8, 10 or 12 bit Wilkinson ADC.

Detector Read-Out	MAPMT, SiPM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger on 1/3 photo-electron with a 10^6 PM gain or 50 fC
Timing Resolution	60ps RMS on single photo-electron, threshold 1/3 of photo-electron
Dynamic Range	5 pC (10^6 PM gain), Integral Non Linearity: 2% up to 5 pC
Packaging & Dimension	TFBGA353, ~~PQFP240~~ discontinued
Power Consumption	3.5 mW /ch, power supply= 3.3V
Inputs	64 current inputs
Outputs	64 trigger outputs Wired OR of the 64 triggers for each of the 2 discriminators 1 multiplexed analog charge output that can be daisy chained 1 digital charge measurement (8, 10 or 12 bits)
Internal Programmable Features	gain adjustment between 0 and 2 over 8 bits for each input preamp, trigger threshold adjustment (10bits), analog and digital charge measurement, 64 trigger outputs, 64 trigger masks

They are using Maroc 3A

CERN (ATLAS luminometer)
Jefferson lab (CLASS12)
Industrial applications under NDA

More about Maroc 3A

Contact Jean-Baptiste CIZEL
Web https://www.weeroc.com
Email maroc@weeroc.com
Phone +33 1 69 59 69 27

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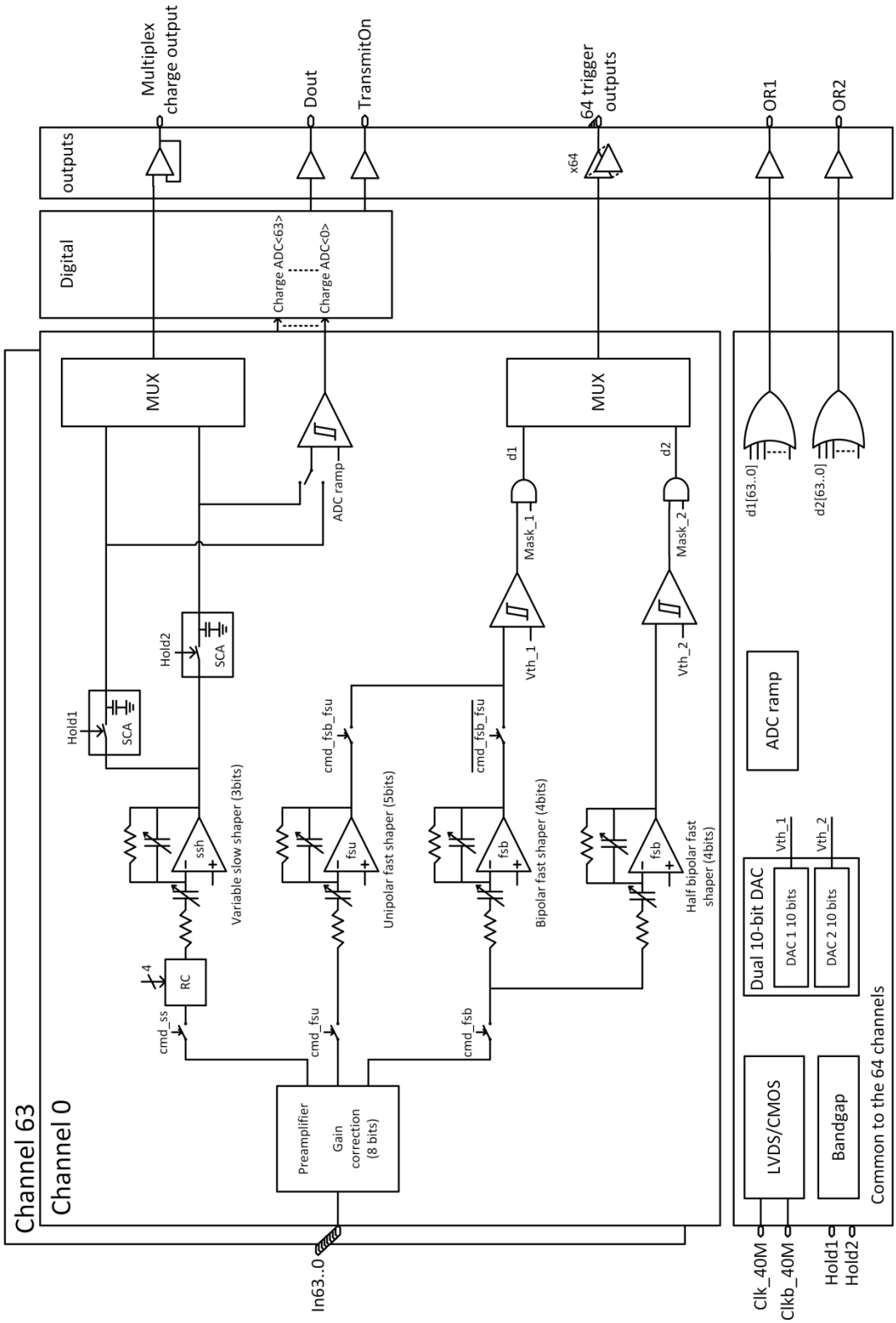
Maroc 3A

Photomultiplier-tubes read-out chip



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Catiroc 1

Large-Photomultiplier-Arrays Read-Out Chip

CATIROC 1 is a 16-channel front-end ASIC designed to readout photomultiplier tubes (PMTs) in large scale applications such as water Cerenkov experiments. The concept of the ASIC is to combine an auto-trigger chip to 16 PMTs to obtain an autonomous macro-cell for large area of detection.

An adjustment of the gain of each channel compensates for the gain variation of the PMTs and allows using only one HV cable for the 16 PMTs. In the ASIC, the 16 channels are totally independent. In each channel, the auto-trigger starts the charge and time measurements which are then converted and stored. Only the hit channels are read out by one serialized output. The time measurement is done by a 26-bit counter at 40 MHz for the coarse time and a Time to Amplitude Converter (TAC) for the fine time, giving a resolution of 200ps RMS. The charge measurement is done by a dual gain preamplifier followed by a shaper with variable shaping times (25 ns, 50 ns or 100 ns). Charge and fine time values are converted by a 10 bit ADC.

Moreover CATIROC 1 can be used as an analogue front-end ASIC for PMTs. The 16 triggers and 16 shapers output can be used in an application specific optimized front-end board.

Detector Read-Out	PMT, PMT array
Number of Channels	16
Signal Polarity	Negative
Sensitivity	Trigger on one third of photo-electron on each channel
Timing Resolution	200ps RMS on single photo-electron
Dynamic Range	400 photo-electrons (10^6 PMT gain) Integral Non Linearity 1% up to 400 p-e
Packaging & Dimension	TQFP208
Power Consumption	Power supply: 3.3V 21mW/ch.
Inputs	16 voltage inputs
Outputs	16 trigger outputs 16 shaper output 1 or of the 16 trigger output 1 serialized digital data output (50bits/channel)
Internal Programmable Features	16 channel gain adjustment (16x8bits), trigger and gain threshold adjustment (2x10bits), charge measurement tuning, 16 trigger masks, channel by channel trigger output enable.

They are using Catiroc 1

JUNO experiment
WA105 collaboration

More about Catiroc 1

Contact Salleh Ahmad
Web https://www.weeroc.com
Email catiroc@weeroc.com
Phone +33 1 69 59 69 27

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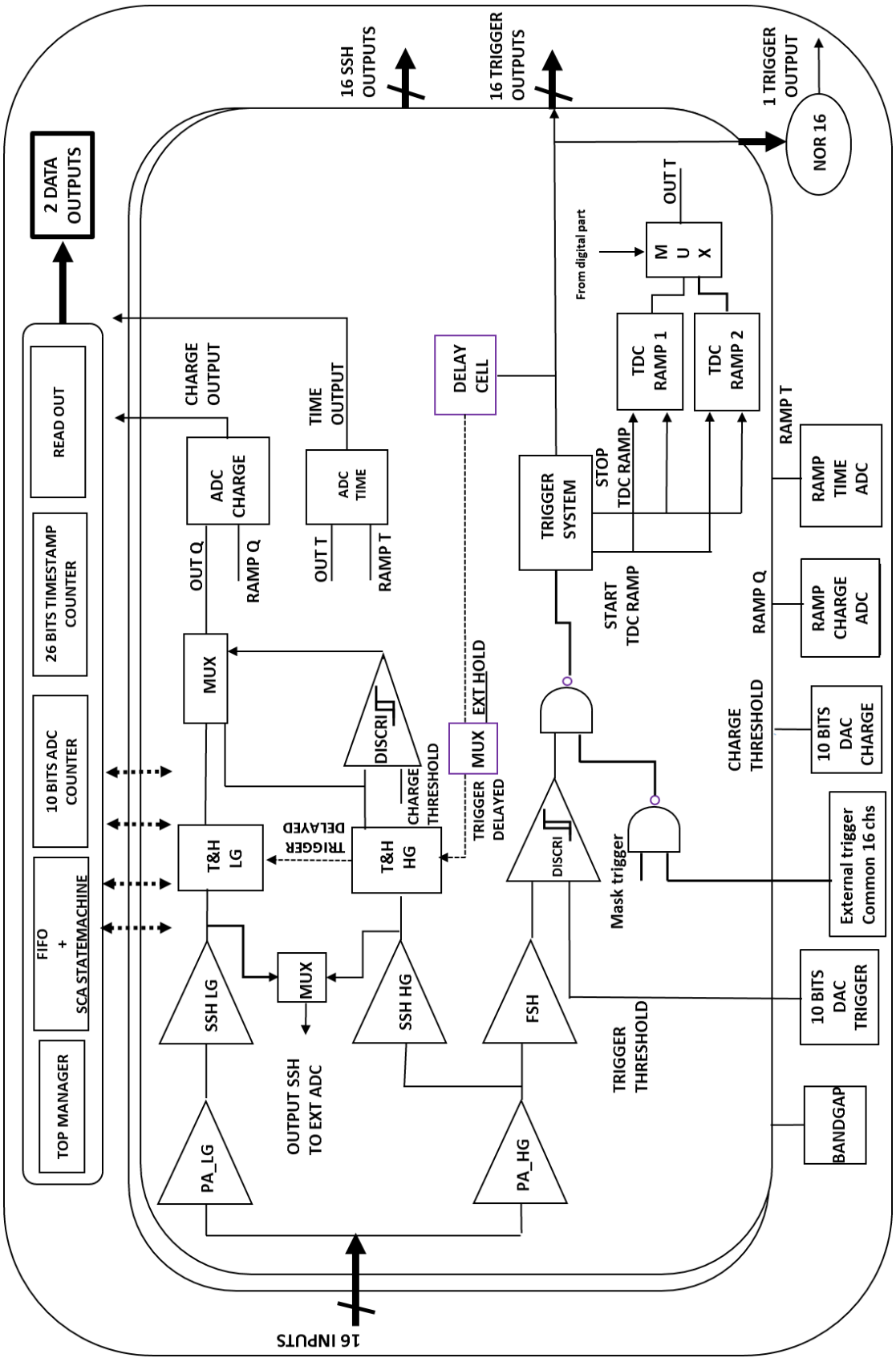
Catiroc 1

Large-Photomultiplier-Arrays Read-Out Chip



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Citiroc 1A

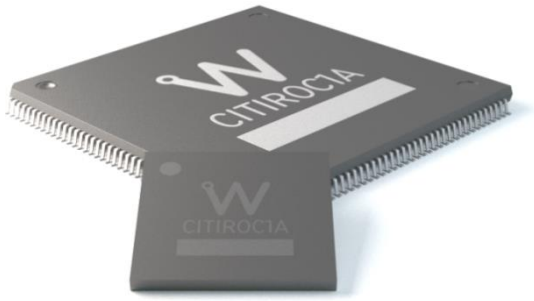
Scientific instrumentation SiPM read-out chip

Citiroc 1A is a 32-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for scientific instrumentation application.

Citiroc 1A allows triggering down to 1/3 pe and provides the charge measurement with a good noise rejection. Moreover, Citiroc 1A outputs the 32-channel triggers with a high accuracy (better than 100 ps).

An adjustment of the SiPM high-voltage is possible using a channel-by-channel DAC connected to the ASIC inputs. That allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs. Citiroc 1A can be calibrated using a unique calibration signal.

Timing measurement better than 100 ps RMS jitter is possible along with 1% linearity energy measurement up to 2500 p.e. The power consumption 225mW with all stages on.



Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 100 ps RMS on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ 10^6 SIPM gain
Packaging & Dimension	TQFP 160 – TFBGA353
Power Consumption	225mW – Supply voltage : 3.3V
Inputs	32 voltage inputs with independent SiPM HV adjustments
Outputs	32 trigger outputs 2 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger output (Trigger OR)
Internal Programmable Features	32 HV adjustment for SiPM (32x8bits), Trigger Threshold Adjustment (10bits), channel by channel gain tuning, 32 Trigger Masks, Trigger Latch, internal temperature sensor

They are using Citiroc 1A

INAF – IASF (CTA experiment)
CERN (Baby mind experiment)

More about Citiroc 1A

Contact Jean-Baptiste CIZEL
Web https://www.weeroc.com
Email citiroc@weeroc.com
Phone +33 1 69 59 69 27

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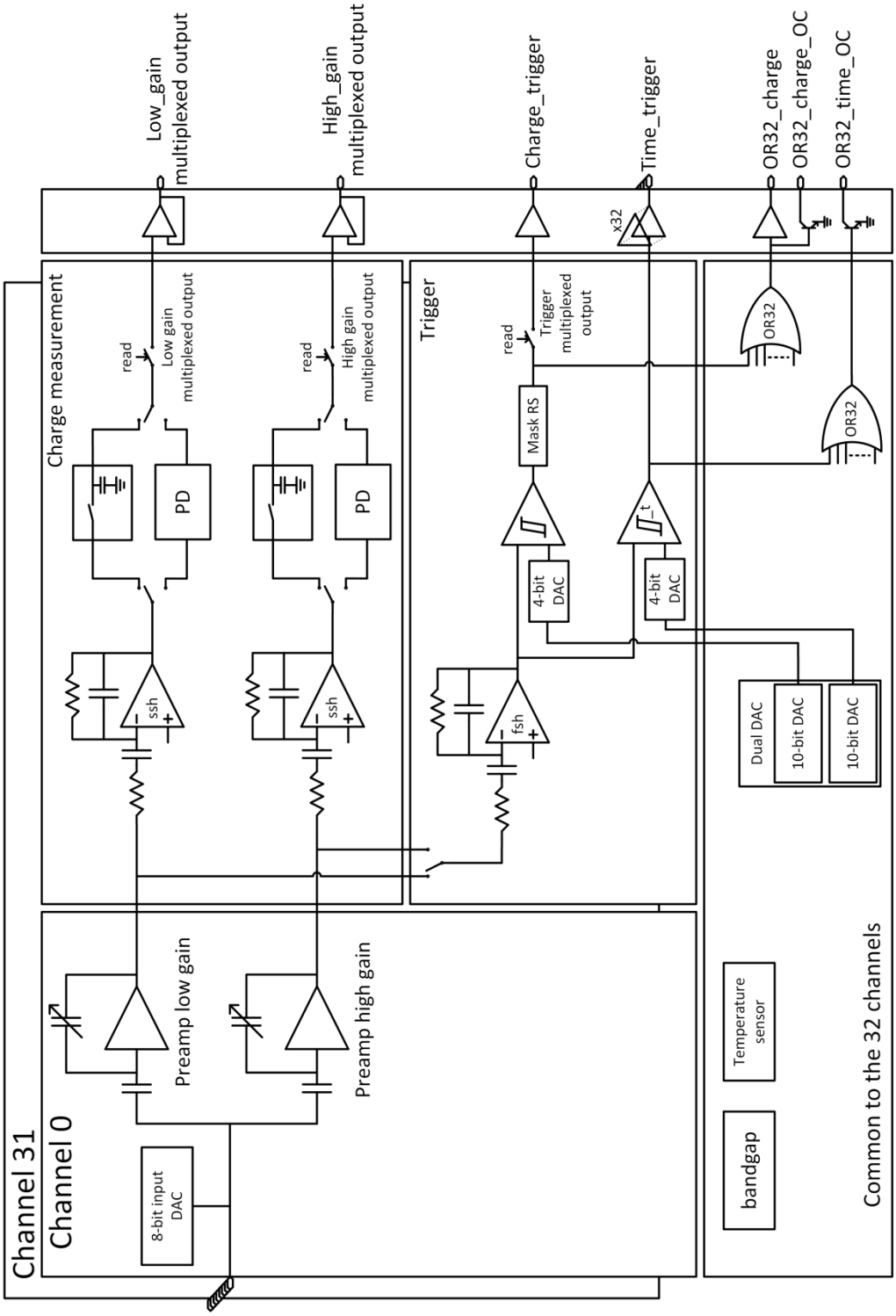
Citiroc 1A

Scientific instrumentation SiPM read-out chip



SSH – Slow Shaper ; FSH – Fast Shaper; PD – Peak Detector

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Petiroc 2A

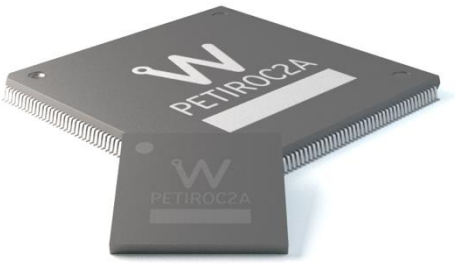
SiPM read-out for time-of-flight PET

Petiroc 2A is a 32-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) with both polarities for particle time-of-flight measurement applications. Petiroc 2A combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 40ps-bin TDC.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 6 mW/channel, excluding buffers used to output the analogue signals. The main application of Petiroc 2A is PET time-of-flight prototyping but it can also be used for any application that requires both accurate time resolution and precise energy measurement.



Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal TDC
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e
Packaging & Dimension	TQFP208 – TFBGA353
Power Consumption	Power supply: 3.3V 192mW Analogue core (excluding analogue outing buffer), 6mW/ch
Inputs	32 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 40ps bin) 32 trigger outputs 1 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger outputs (Trigger OR on 32 channels, 2 levels)
Internal Programmable Features	32 HV adjustment for SiPM (32x8b), trigger threshold adjustment (10b), charge measurement tuning, 32 trigger masks, internal temperature sensor, trigger latch

They are using Petiroc 2A

Industrial applications
Cannot be disclosed

More about Petiroc 2

Contact Jean-Baptiste CIZEL
Web https://www.weeroc.com
Email petiroc@weeroc.com
Phone +33 1 69 59 69 27

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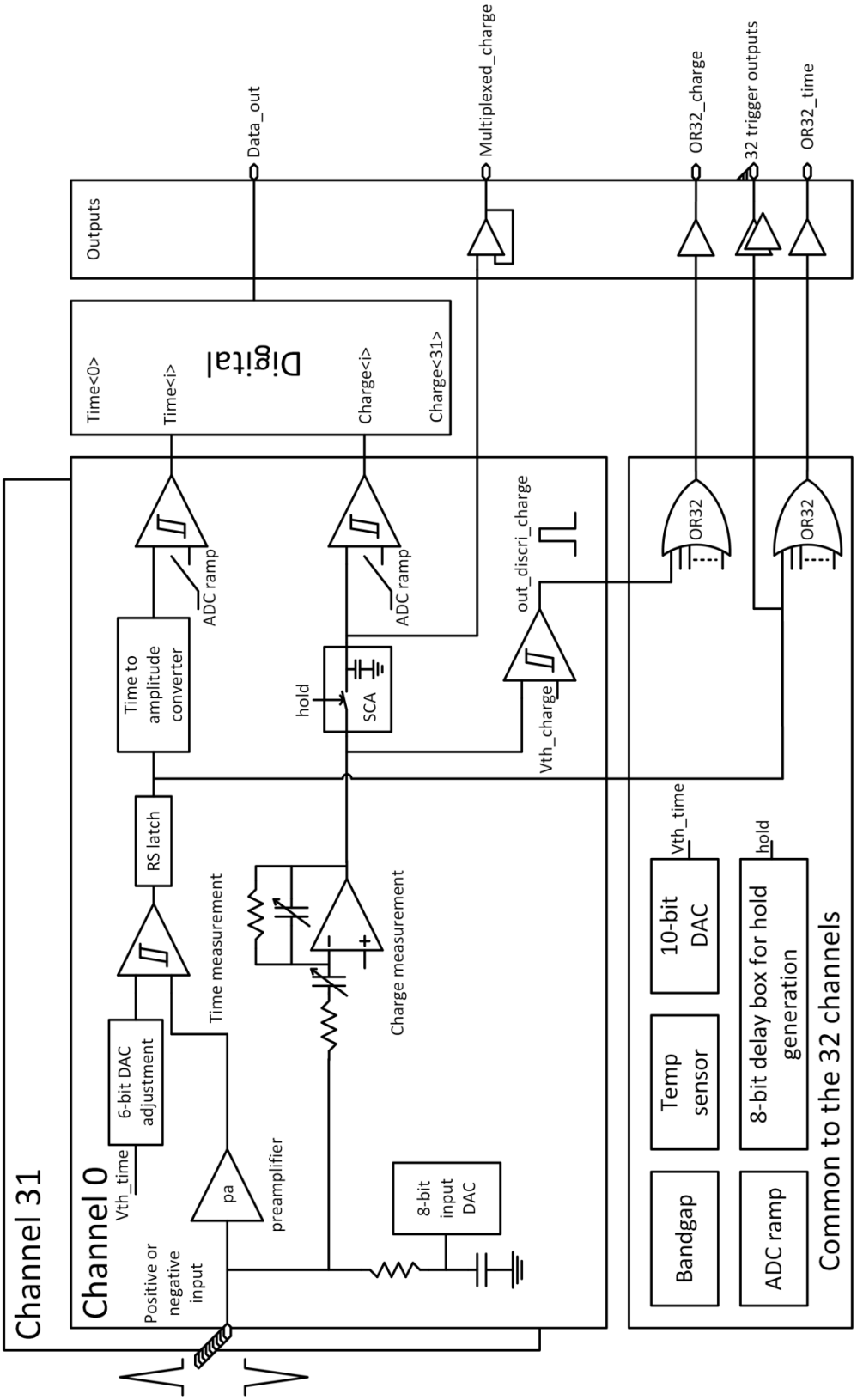
Petiroc 2A

SiPM read-out for time-of-flight PET



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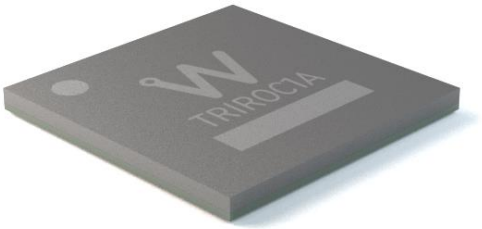
Triroc 1A

All-in-one SiPM read-out for multimodal PET inserts

Triroc 1A is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) with both polarities for particle time-of-flight measurement applications. Triroc 1A combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 30ps-bin TDC.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.



An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 10 mW/channel, excluding buffers used to output the signals. The main application of Triroc 1A is PET time-of-flight but it can also be used for any application that requires both accurate time resolution and precise energy measurement. Triroc 1A is available in naked dies or BGA packaging (12x12mm, 353 balls).

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	88 ps RMS
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging	BGA (12x12mm, 353 balls)
Power Consumption	Power supply: 3.3V 10mW/ch
Inputs	64 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 30ps bin) 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), trigger threshold adjustment (10bits), charge measurement tuning, ADC Track & Hold/Peak Sensing, 64 trigger masks, internal temperature sensor, trigger latch, Power Pulsing

They are using Triroc 1A

Trimage collaboration (PET/IRM/EEG)
Industrial application
Cannot be disclosed

More about Triroc 1A

Contact Salleh Ahmad
Web https://www.weeroc.com
Email triroc@weeroc.com
Phone +33 1 69 59 69 26

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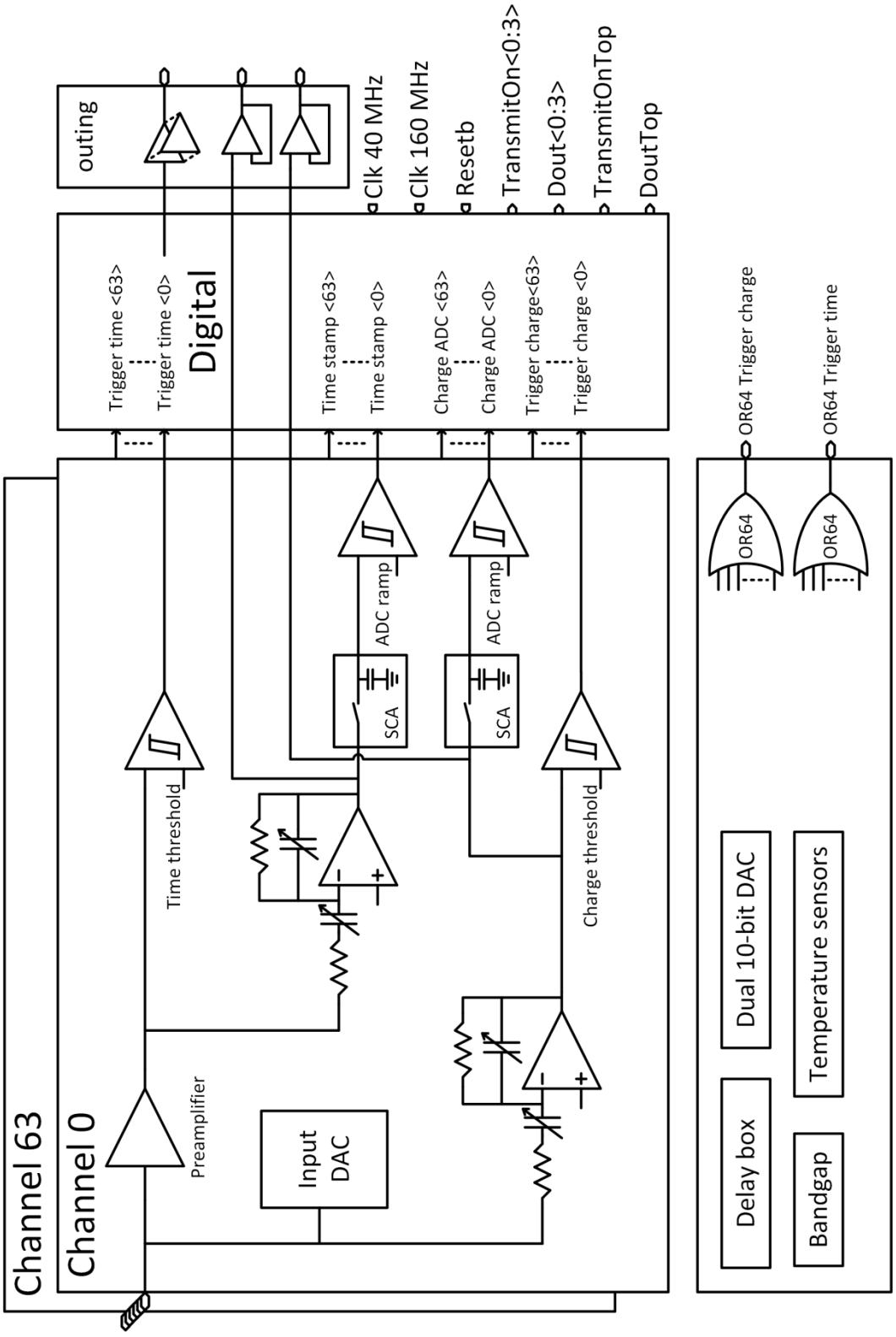
Triroc 1A

All-in-one SiPM read-out for multimodal PET inserts



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Skiroc 2A

PIN Diode and Low Gain Silicium Detector Read-Out Chip

SKIROC 2A is a 64-channel front-end ASIC designed to readout silicon PIN diodes. Each channel is made of a variable-gain and low-noise charge preamplifier followed by two shapers – one with a gain of 1 and the other with a gain of 10 – to provide a charge measurement from 0.2 fC up to 10 pC. A time tagging is performed by a 12-bit TDC ramp. The charges and times are stored in a 15-depth Switched Capacitor Arrays (SCA), the values of which are converted by a multi-channel 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory. The analog value of the charge is also available on an output pin. The trigger chain is composed of a high gain fast shaper and a discriminator and allows each channel to auto trigger down to 0.2 fC. Thresholds of the 64 discriminators are set by a common 10-bit DAC and an individual 4-bit DAC per channel. Each discriminator output is sent to an 8-bit delay cell (delay time tunable between 100 ns and 300 ns) to provide the Hold signal for the SCA cells of the slow channel. The power consumption is 6.2 mW/channel and each stage can be individually shut down when not used. 616 slow control parameters are available to set various configurations and ensure the versatility of the chip.

Detector Read-Out	Si PIN Diodes
Number of Channels	64
Signal Polarity	positive
Sensitivity	Trigger on 0.2fC
Timing Resolution	N/A
Dynamic Range	10 pC, Integral Non Linearity <1%
Packaging & Dimension	BGA 400 (17x17mm)
Power Consumption	6.2 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	1 multiplexed analog charge output 12-bit charge and time measurement Trigger OR of the 64 discriminators
Internal Programmable Features	Common gain adjustment for the input, common trigger threshold adjustment (10 bits) and individual threshold (4 b), 12-bit charge and time measurement, 64 trigger masks, multiplexed analog output

They are using Skiroc 2A

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More about Skiroc 2A

Contact Jean-Baptiste CIZEL
Web https://www.weeroc.com
Email skiroc@weeroc.com
Phone +33 1 69 59 69 27

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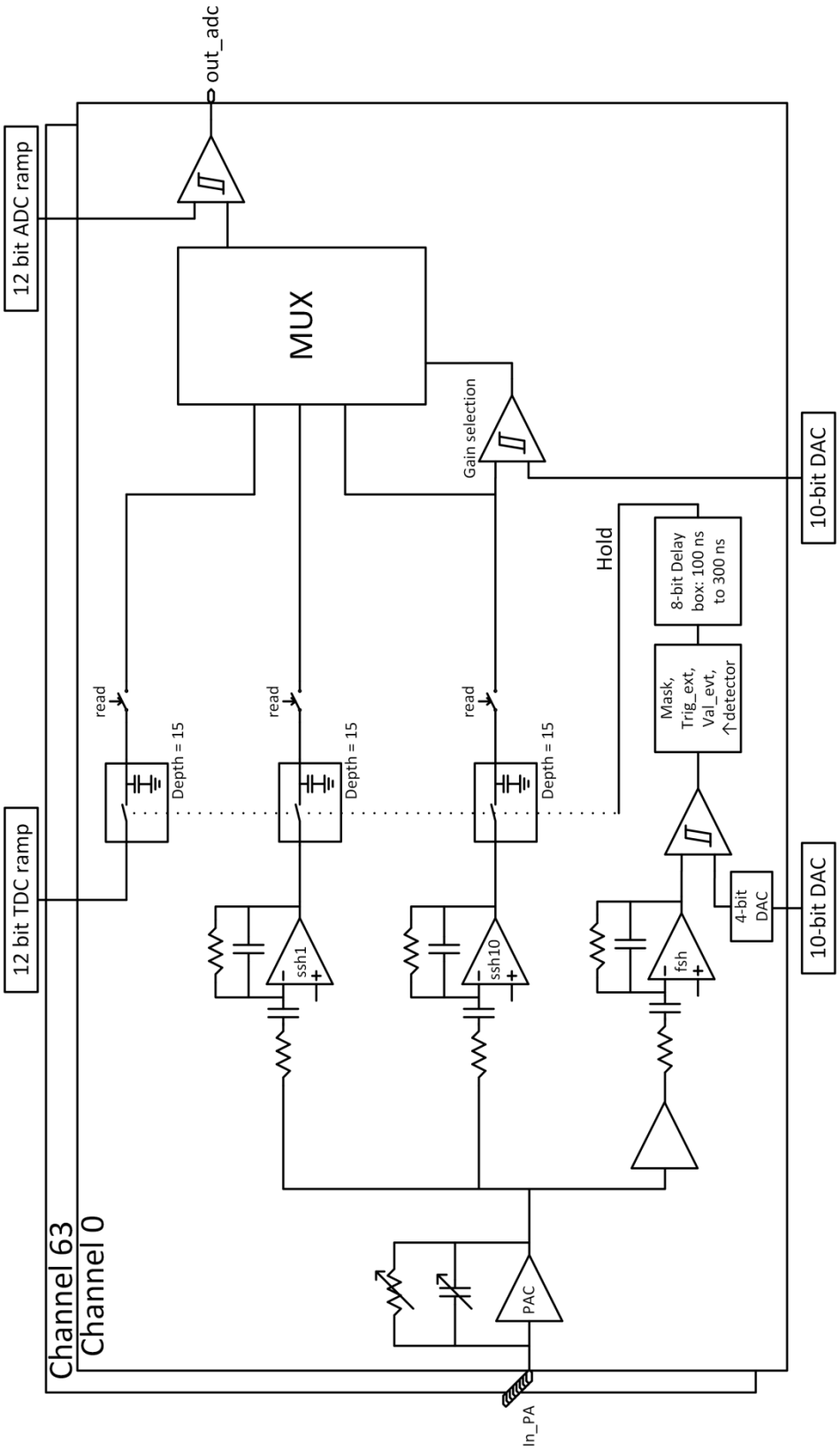
Skiroc 2A

PIN Diode and Low Gain Silicium Detector Read-Out Chip



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Gemroc 1

Micromegas and GEMs semi-digital read-out chip

GEMROC 1 is a 64-channel front-end ASIC designed to readout negative fast (<1ns) and short (<10ns) current pulses from low gain detectors (GEMs, Micromegas, ...). GEMROC 1 provides a semi-digital readout with three thresholds tunable from 1 fC to 500 fC and integrates a 128-deep digital memory to store the 2 x 64 discriminator outputs as well as the timestamp from a 24b counter. The three thresholds are set internally by three 10-bit DACs. The gain of each channel can be tuned individually from 0 to 2 over 8 bits, allowing the compensation of non-uniformity between the 64 detector channels. Each channel can auto trigger down to 1 fC input charge. A multiplexed charge measurement up to 500fC is integrated.

The power consumption is 1.5 mW/channel and the chip can be fully power-pulsed allowing a significant power reduction by disabling unused blocks.

Detector Read-Out	Micromegas, GEM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger 1 fC
Timing Resolution	N/A
Dynamic Range	500 fC
Packaging & Dimension	TQFP160
Power Consumption	1.5 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	2 encoded data outputs per channel streamed out in serial 1 multiplexed charge output 3 multiplexed trigger outputs or 3 trigger OR of the 64 channels
Internal Programmable Features	Trigger threshold adjustment (10bits), 3*64 trigger masks, multiplexed latched trigger or direct OR64 trigger outputs

They are using Gemroc 1

Industrial application (NDA)

More about Gemroc 1

Contact Salleh Ahmad
Web https://www.weeroc.com
Email gemroc@weeroc.com
Phone +33 1 69 59 69 27

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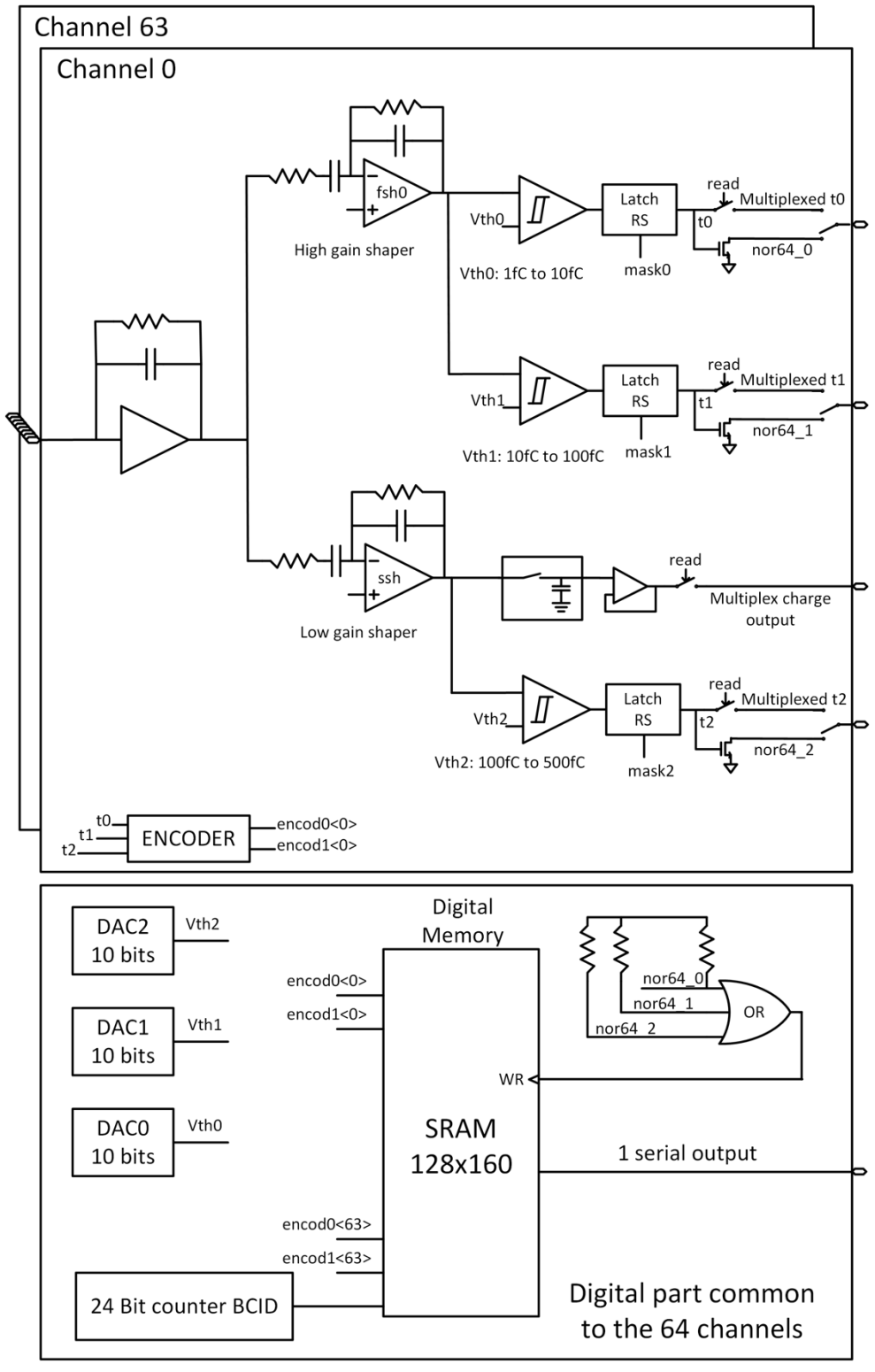
Gemroc 1

Micromegas and GEMs semi-digital read-out chip



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